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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/085,782	02/28/2002	Yueyong Wang	RAMB-01009US0	2045

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VIERRA MAGEN MARCUS HARMON & DENIRO LLP
685 MARKET STREET, SUITE 540
SAN FRANCISCO, CA 94105

EXAMINER	
NGUYEN, MINH T	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 05/27/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application N .	Applicant(s)	
	10/085,782	WANG ET AL.	
	Examin r	Art Unit	
	Minh Nguyen	2816	

-- The MAILING DATE of this communication appears n the cover she t with the corresp ndence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 May 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *10,11,19,20,24 and 25* is/are allowed.

6)☒ Claim(s) *1-8,12-18,21-23 and 26-31* is/are rejected.

7)☒ Claim(s) *9* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 February 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. Applicants' amendment filed on 5/5/03 has been received and entered in the case. Claims 1-31 are pending. The amendments and arguments presented therein overcome the objections and prior art rejections noted in the previous Office Action, and therefore, are withdrawn. New grounds of rejections are needed as set forth below. This action is NON-FINAL.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-8, 12-18 and 28-31 are rejected under 35 U.S.C. 102(b) as being anticipated by US Patent No. 6,111,445, issued to Zerbe et al.

As per claim 1, Zerbe discloses a circuit (Fig. 21), comprising:

a first node 2108 capable to provide a variable first voltage JX;

a second node 2109 capable to provide a variable second voltage JXB;

a first transistor 2316, coupled to the first node (at the drain), having a first gate for providing a first current (through transistor 2316) responsive to a first control voltage (the voltage at the gate of 2316) being applied to the first gate;

a second transistor 2318, coupled to the second node 2109 (at the drain), having a second gate for providing a second current responsive to a second control voltage being applied to the second gate;

a first control circuit (2313, 2312, 2315), coupled to the first gate and the second node 2109 (as shown), for providing the first control voltage responsive to the variable second voltage JXB (the first control voltage is provided at the gate of 2316 responsive to the second variable voltage JXB); and,

a second control circuit (2314, 2311, 2317), coupled to the second gate and the first node 2108 (as shown), for providing the second control voltage (at the gate of transistor 2318) responsive to the first variable voltage JX (the second control voltage is provided at the gate of 2318 responsive to the first variable voltage JX).

As per claim 2, the circuit of claim 1, wherein the first variable voltage is different from the second variable voltage (see Fig. 7 and also the specification).

As per claim 3, the circuit of claim 1, wherein the first and second transistors operate in a saturation region (since the Zerbe's first and second transistors have all the connections and configurations as discussed herein above, the Zerbe's first and second transistors must be assumed to operate in saturation region also. It is further noted that if the Applicants argue that transistors 2316 and 2318 do not operate in a saturation region, claims 1 and 3 would be rejected under 112, first paragraph in the next Office Action on the ground that the claims lack of essential structural and/ or elements relationship for the recited first and second transistors to operate in saturation region, i.e., if the claimed circuit has the same structure as the reference

circuit, the result must be the same which is the first and second transistors in the Zerbe reference must also be operated in the saturation region).

As per claim 4, the circuit of claim 1, wherein the circuit further comprises:

a third transistor 2311, coupled to the first node (at the gate), having a third gate coupled to the first node (2108), for providing a third current (the current flows through transistor 2108) responsive to the first variable voltage JX; and,

a fourth transistor 2312, coupled to the second node (at the gate), having a having a fourth gate coupled to the second node (as shown), for providing a fourth current (the current flows through transistor 2312) responsive to the second variable voltage JXB.

As per claim 5, the circuit of claim 4, wherein the first current approximately equals the fourth current and the third current approximately equals the second current (the recited limitation is met because they are current mirrors).

As per claim 6, the circuit of claim 1, wherein the first variable voltage and the second variable voltage are obtained from a clock signal (since nodes 2108 and 2109 can receive any signal which includes signal from a clock signal, the recited limitation is met).

As per claim 7, the circuit of claim 6, wherein the clock signal has an amplitude of greater than approximately 400 mv (the recited limitation is met because the circuit of claim 6 clearly can receive the clock signal has an amplitude of greater than approximately 400 mv).

As per claim 8, the circuit of claim 4, wherein the first current, the second current, the third current and the fourth current are used to provide a duty cycle correction signal. The recited limitation is merely an intended use and is met since the Zerbe circuit can be used for this purpose.

As per claim 12, the circuit of claim 1, wherein the circuit is a cross-coupled load with a built-in current mirrors circuit (as shown they are cross-coupled and current mirrors configuration) used in a double data rate receiving circuit for improving a clock signal (this limitation is merely an intended use, no patentable weight is given accordingly).

As per claim 13, the circuit of claim 1, wherein the circuit is in a memory device. This limitation is merely an intended use, no patentable weight is given accordingly.

As per claim 14, the circuit of claim 1, wherein the circuit is in a memory device controller (the claim is rejected for the same reason noted in claim 13).

As per claim 15, Zerbe discloses a circuit for correcting a duty cycle of a clock signal (Fig. 21), comprising:

a first node 2108 for providing a first variable voltage JX representing the clock signal;

a second node 2109 for providing a variable second voltage JXB representing the clock signal;

a first transistor 2316, coupled to the first node (at the drain), having a first gate for providing a first current (through transistor 2316) responsive to a first control voltage (the voltage at the gate) being applied to the first gate, wherein the first transistor is operating in a saturation region (transistor 231 clearly can operate in saturation region);

a second transistor 2318, coupled to the second node (at the drain), having a second gate for providing a second current responsive to a second control voltage being applied to the second gate, wherein the second transistor is operating in a saturation region;

a first control circuit (2315, 2313 and 2312), coupled to the first gate and the second node (as shown), for providing the first control voltage responsive to the variable second voltage (see claim 1 for further explanation); and,

a second control circuit (2317, 1314, 2311), coupled to the second gate and the first node, for providing the second control voltage responsive to the variable first voltage, wherein the first voltage is greater than the second voltage (see claim 1).

As per claim 16, the circuit of claim 15, wherein the circuit further comprises:

a third transistor 2311, coupled to the first node, having a third gate coupled to the first node, for providing a third current responsive to the first variable voltage; and,

a fourth transistor 2312, coupled to the second node, having a fourth gate coupled to the second node, for providing a fourth current responsive to the second variable voltage.

As per claims 17-18, these claims are rejected for the same reasons noted in claims 5 and 8, respectively.

As per claim 28, this claim is merely a method to operate the circuit having elements and connections discussed in claim 1 above, since Zerbe teaches the circuit, he inherently teaches the recited method.

As per claims 29-31, these claims are rejected for the same reasons noted in claims 4-5 and 8, respectively.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 21-23 and 26-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 6,111,445, issued to Zerbe et al.

As per claim 21, Zerbe discloses a load circuit (Fig. 21) in a phase interpolator circuit (Fig. 5) wherein the load circuit includes

a first node 2108 for providing a variable first voltage JX;

a second node 2109 for providing a variable second voltage JXB;

a first transistor 2316, coupled to the first node (the drain), having a first gate for providing a first current (the current flows through transistor 2316) responsive to a first control voltage (the voltage at the gate of 2316) being applied to the first gate;

a second transistor 2318, coupled to the second node 2109 (the drain), having a second gate for providing a second current responsive to a second control voltage being applied to the second gate;

a first control circuit (see claim 1), coupled to the first gate and the second node (as shown), for providing the first control voltage responsive to the variable second voltage JXB; and,

a second control circuit (see claim 1), coupled to the second gate and the first node 2108 (as shown), for providing the second control voltage (at the gate of transistor 2318) responsive to the variable first voltage JX.

Zerbe further discloses that his interpolator circuit is used in a DLL or PLL circuit (column 1, lines 15-16).

Zerbe does not explicitly disclose that the interpolator circuit is in a receive circuit wherein the receive circuit is coupled to a transmit circuit as called for in the claim.

The examiner takes Official Notice the fact that in a memory system, a receiver circuit coupled to a transmit circuit to receive the signal from the transmit circuit is old and well-known in the art. Specific example would be the transmit circuit is a memory controller which exists in every computer system which transmit data and control signals to control and access data in the memory modules and the receiver circuit includes a PLL or DLL circuit.

It would have been obvious to one skilled in the art at the time of the invention was made to include the Zerbe's interpolator circuit in the PLL circuit in the receiver circuit.

The motivation and /or suggestion for doing so would have been obvious since by incorporating the Zerbe's interpolator circuit, noise immunity could be improved (column 1, lines 45).

Therefore, it would have been obvious to include the interpolator circuit taught by Zerbe in a conventional receiver circuit to obtain the invention specified in the claim.

As per claims 22-23, these claims are rejected for the same reasons noted in claims 4-5, respectively.

As per claim 26, the recited limitation is met since in a memory system, the transmit circuit is included in a memory controller and the receive circuit is included in a memory device.

As per claim 27, since the Zerbe circuit is for improving noise immunity, the recited limitation is met.

Response to Arguments

4. Applicant's arguments with respect to the claims have been considered but are moot in view of the new ground(s) of rejection.

Allowable Subject Matter

5. Claims 10-11, 19-20 and 24-25 are allowed for the reasons noted in the previous Office Action.

6. Claim 9 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim 9 is allowable because the prior art of record fails to disclose or suggest a circuit which includes first, second, third and fourth transistors connected as recited and the recited four transistors are n-type transistors. Zerbe teaches the first and second are p-type and the third and fourth are n-type.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Minh Nguyen whose telephone number is 703-306-9179. The examiner can normally be reached on Monday, Tuesday, Thursday, Friday 7:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 703-308-4876. The fax phone numbers for the

organization where this application or proceeding is assigned are 703-872-9318 for regular communications and 703-872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Minh Nguyen
Primary Examiner
Art Unit 2816

MN
May 26, 2003